REMARKS:

Claims 1-19 were presented for examination and were pending in this application. In an Official Action dated January 13, 2005, claims 1-11 were rejected and claims 12-19 were withdrawn from consideration by Examiner. Applicants thank Examiner for examination of the claims pending in this application and addresses Examiner's comments below.

Applicants thank Examiner for considering the references submitted in the Information Disclosure Statement (IDS) filed November 4, 2004 by Applicants. However, Applicants note that two additional IDSs were filed for which the Examiner has not provided an indication of having considered the references cited therein. Applicants filed an IDS on December 10, 2004, which is reflected in PAIR and an earlier filed IDS on July 30, 2004, which is not reflected in PAIR. Copies of the filing documents associated with the July 30th IDS are attached herewith, including the Office's stamped Receipt Postcard. Applicants kindly request consideration of the references cited in these two IDSs and written indication thereof on the corresponding PTO/SB/08A forms.

Applicants herein amend claims 1, 5, 6, 8, and 11. These changes are believed not to introduce new matter, and their entry is respectfully requested. The claims have been amended to expedite the prosecution of the application in a manner consistent with the Patent Office Business Goals, 65 Fed. Reg. 54603 (Sept. 8, 2000). In making these amendments, Applicants have not and do not narrow the scope of the protection to which Applicants consider the claimed invention to be entitled and do not concede that the subject matter of such claims was in fact disclosed or taught by the cited prior art. Rather, Applicants reserve the right to pursue such protection at a later point in time and merely seek to pursue protection for the subject matter presented in this submission.

Based on the above Amendment and the following Remarks, Applicants respectfully request that Examiner reconsider all outstanding objections and rejections, and withdraw them.

Response to Restriction Requirement

In the 1st and 2nd paragraphs of the Office Action the claims were restricted into two groups, claims 1-11 and claims 12-19. Applicants elect with traverse claims 1-11 as Examiner constructively elected. However, Applicants respectfully submit that restriction of claims 12-19 and their withdrawal is improper. Applicants thank Examiner Harkness for kindly discussing this restriction requirement and as agreed summarize the discussion with Examiner and provide the table below.

A restriction requirement is proper where more than one invention is claimed and the inventions are independent or distinct, and failure to restrict imposes a serious burden on the Examiner. See MPEP at 803. In the instant case, the two sets of claims each do not contain a distinct invention, neither does the failure to restrict impose a serious burden.

> The term "distinct" means that two or more subjects as disclosed are related, for example, as combination and part (subcombination) thereof, process and apparatus for its practice, process and product made, etc., but are capable of separate manufacture, use, or sale as claimed, AND ARE PATENTABLE (novel and unobvious) OVER EACH OTHER (though they may each be unpatentable because of the prior art). It will be noted that in this definition the term related is used as an alternative for dependent in referring to subjects other than independent subjects.

See MPEP § 802.01.

This restriction was essentially based on the argument that "[i]ncluding all of this information inside of the control and status register [of claims 12-19] is an entirely different invention that includes new matter, and changes the scope for the originally claimed

invention." The "all of this information" that is included in the control and status register of claims 12-19 is described by Examiner as (1) a set of thread selection bits for indicating a source context of a source thread from which source operands are obtained to be used in a current thread and (2) a set of thread selection bits for indicating a destination context of a destination thread to which the results are to be written.

Applicants respectfully submit that claims 12-19 do not introduce any new matter and is not directed to an invention that is "distinct" from that originally claimed in claim 1. Claim 1, as originally filed, included a control status register with very similar information as shown in the following table:

In original Claim 1	In Claim 12
A first control status register	A control and status register having sets of thread selection bits
for identifying a first target set of data storage devices from which a first source operand of a first fetched instruction is to be retrieved from	for indicating to the processor a source context of a source thread from which source operands are obtained to be used in a currently executed thread
for identifying a second target set of data storage devices to which a first result of a first executed instruction is stored	for indicating to the processor a destination context of a destination thread to which execution results of the currently executed thread are written

Accordingly, Applicants kindly request withdrawal of the restriction requirement and consideration of claims 12-19 as part of the present application.

Response to Rejection Under 35 USC 102(e)

In the 3rd paragraph of the Office Action, Examiner rejects claims 1-11 under 35 USC § 102(e) as allegedly being anticipated by U.S. Patent No. 6,542,991to Joy et al. ("Joy"). This rejection is now traversed.

Claim 1 has been amended to clarify the ability to interact between all the threads in the multithreaded computer system as follows:

> wherein at least said first set of data storage devices includes a control status register for identifying a first target set of data storage devices from which a first source operand of a fetched instruction is to be retrieved and for identifying a second target set of data storage devices to which a first result of an executed instruction is to be stored, wherein at least one of said first or said second target set of data storage devices is not included in the first set of data storage devices;

The ability to identify a target set of storage devices for retrieving operands and another set for storing execution results where the target sets of storage devices are associated with different threads executing in the multithreaded processor (i.e., "wherein at least one of said first or said second target set of data storage devices is not included in the first set of data storage devices") provides the flexibility to, for example, selectively change states of variables associated with other threads by a controlling or managing program thread.

Conversely, Joy's windows do not provide the ability to specify a target sets for retrieving operands and storing results. Joy's windows simply provide the ability to "pass parameters on function calls without having to store and retrieve data through the stack" (Joy, col. 30, lines 55-61). The mechanism for doing this does not include identifying target sets of data storage devices, "wherein at lease one of said first or said second target set of data storage devices is not included in the first set of data storage devices" because the INS and OUTS in each window are simply shared registers that belong to both windows at the same time. As Joy explains with respect to FIG. 17A (repeatedly cited by Examiner), it "illustrates sharing of registers among adjacent windows." (Joy, col. 29, lines 54-64).

> Overlapping windows allow a calling function to send parameters to a receiver without additional load and store operations. A calling function has a current calling window 1710 that uses "OUTS" registers

> 1712 to pass parameters to and adjacent current receiver window 1720 where the registers become "INS" registers 1722 for the receiver.

Id. Thus, in Joy's windows technique there is no identification of different sets of target data storage devices for retrieving and storing information, the same registers are "OUTS" with respect to a "calling window" and become "INS" with respect to the adjacent receiver window.

Accordingly, Joy does not teach the thread interaction in a multithreaded processor as recited in the claimed invention of claim 1.

Similarly, claims 5 and 11 recited a method and apparatus for executing instructions that enable the thread interaction of the claimed invention. The instructions include determining a context for source data registers and storing in destination data registers associated with a context. As described above, this is not described in Joy because in Joy there is no ability to select contexts for source operands or for storing results. The INS and OUTS register is the shared register between adjacent windows. Each window is associated with a context at the time the context is created. The interaction between contexts is limited to the shared register between adjacent windows. Thus, there is no need to indicate a source or destination context, the source and destination contexts are always given by the current window since only the adjacent context can be interacted with through a given shared register.

Accordingly, for at least these reasons, claims 1, 5, and 11, and their dependent claims 2-4 and 6-10 are patentably distinguishable over the cited reference. Therefore, Applicants respectfully request that Examiner reconsider the rejection, and withdraw it.

Conclusion

In sum, Applicants respectfully submit that claims 1 through 19, as presented herein, are patentably distinguishable over the cited references (including references cited, but not applied). Therefore, Applicants request reconsideration of the basis for the rejections to these claims and request allowance of them.

In addition, Applicants respectfully invite Examiner to contact Applicants' representative at the number provided below if Examiner believes it will help expedite furtherance of this application.

Respectfully Submitted,
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Date: 3/14/2005 By: _____

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